

16. (New) The frame of Claim 15 wherein said frame defines at least one cavity therein, said lead frames and the corresponding said semiconductor devices being disposed in said cavity, said frame further comprising molding compound disposed in said cavity so as to encapsulate upper sides of said semiconductor devices and lower sides of said die pads.

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#### REMARKS

The Office Action dated February 15, 2002 has been carefully reviewed, and the application is amended herein in a sincere effort to place same in condition for allowance. Reconsideration of the application is respectfully requested.

The specification is amended herein to correct minor typographical and grammatical-type errors. The title is also amended herein.

Applicants propose that Figures 1-6 be amended as indicated in red on the enclosed drawing sheets. The proposed drawing amendments are explained in detail on the Letter to the Official Draftsperson.

A certified copy of the priority document is submitted herewith, and written acknowledgement of the receipt of same is requested. A Supplemental Declaration is also enclosed wherein the title thereon corresponds to the title on the specification as originally filed.

An Information Disclosure Statement is also submitted herewith, along with the prior art consideration fee. Consideration of the references listed on Form PTO-1449 is respectfully requested.

Claims 1 and 2 stand rejected under 35 USC 102 as anticipated by Mclellan (U.S. Patent No. 6 229 200). Figures 6a through 8b of Mclellan illustrate a lead frame for a double-row SSPLCC. Mclellan teaches that a half-etched portion 606 is provided between an annular row of inner leads 603 and an annular row of outer leads 602, and that lead frame

600 is cut along portion 606 to sever the inner and outer leads from one another. The half-etched portion 606 is provided in order to allow a clearance which prevents damage to wire bonds 801 between the semiconductor die 803 and outer leads 602. The line 703 which extends along the outer periphery of lead frame 600 defines the singulation path for forming individual semiconductor packages.

Claim 1 is amended herein for clarification purposes only, and is directed to a frame for semiconductor packages including plural lead frames arranged in a matrix through grid-leads, "the grid-leads having terminals which project therefrom and terminals of adjacent pairs of lead frames are connected to one another at respective connection areas...wherein thin parts are formed adjacent roots of individual terminals, the terminal roots being disposed in the respective connection areas defined between interconnected pairs of terminals of adjacent lead frames". Mclellan does not teach or suggest thin parts formed adjacent line 703, which is the area where the lead frame 600 would be connected to adjacent lead frames. While Mclellan does show (in other figures than those mentioned above) a matrix of interconnected lead frames, Mclellan does not provide a thin part adjacent roots of the outer terminals 602 disposed in a connection area defined between outer terminals 602 and outer terminals 602 of an adjacent lead frame (i.e. at line 703). Indeed, Mclellan does not even show the lead frame 600 in a connected state with other lead frames.

The Examiner states that Claims 1 and 2 do not distinguish over Mclellan regardless of the process used to cut the semiconductor devices into individual semiconductor packages. However, Claim 1 is directed to a **frame** including a plurality of lead frames, and the configuration of the respective lead frames prior to such cutting which results in individual semiconductor packages. In this regard, the

purpose of providing the thin parts recited in Claim 1 is to maintain a sufficient distance between adjacent pairs of terminals of the individual lead frames of the frame, which is an advantageous frame construction which minimizes the remainder of metal at the terminal roots after the frame is cut to divide the semiconductor packages. Mclellan does not teach or suggest this overall frame configuration.

Accordingly, Claim 1 is believed allowable over Mclellan. Claim 2 is amended for clarification purposes only. Claim 2 depends from Claim 1 which is believed allowable for the reasons presented above. Further, Claim 2 recites additional features which further distinguish over Mclellan.

Claim 3 stands rejected under 35 USC 103 as obvious over Mclellan '200 and Ebihara (U.S. Patent No. 5 753 535). Ebihara discloses a lead frame with a body 1 (or die pad) which mounts a semiconductor chip 4 thereon as shown in Figure 6. The body 1 is a multi-layer construction. Through holes 14 are formed in bottom layer 11, and hollow spaces 15 are formed in the intermediate layer 12 which communicate with the holes formed in bottom layer 11. The holes 14 and spaces 15 are provided to improve the bonding strength between the body 1 and the sealing resin.

Claim 3 is amended for clarification purposes only, and is directed to a frame for semiconductor packages including plural lead frames arranged in a matrix through grid-leads, "the grid-leads having terminals which project therefrom and terminals of adjacent pairs of lead frames are connected to one another at respective connection areas...wherein hollows are formed adjacent roots of individual terminals, the terminal roots being disposed in the respective connection areas defined between interconnected pairs of terminals of adjacent lead frames". As acknowledged by the Examiner, Mclellan does not show such hollows. Ebihara does not teach or suggest providing hollows adjacent roots of individual

terminals (i.e. adjacent terminals 1'). As discussed above, Ebihara provides holes and hollows in the die pad or body 1 which mounts the semiconductor chip 4, and does not in any way suggest the desirability of providing hollows adjacent terminals 1'. Accordingly, if the teachings of Mclellan and Ebihara are combined, the result would be to provide the die-attach pad 601 of Mclellan with the holes 14 and hollows 15 taught in Ebihara. Claim 3 is therefore believed allowable over Mclellan and Ebihara.

Claims 4-16 are added herein. Independent Claim 4 is directed to a frame for forming individual semiconductor packages, and recites "each said lead frame having a metal lead which defines a boundary between said lead frame and an adjacent lead frame, and pairs of terminals project in opposite directions from each said lead disposed between an adjacent pair of lead frames, wherein roots of the respective pairs of interconnected terminals disposed closely adjacent the corresponding lead and projecting outwardly therefrom each have a reduced thickness such that a maximum distance is maintained between laterally adjacent pairs of roots of individual lead frames". As discussed above, Mclellan shows a single lead frame in Figures 6a-8b, and does not teach or suggest that the roots of terminals 602 are of a reduced thickness adjacent line 703, which is the area where the lead frame 600 would be connected to adjacent lead frames. Claim 4, and Claims 5-10 which depend therefrom are therefore believed allowable as presented.

Claims 5-10 also include additional features which further distinguish over Mclellan. For example, Claim 6 recites "said roots of each interconnected pair of terminals of interconnected lead frames and a portion of the corresponding said lead disposed between said roots are half-etched". Mclellan discloses no such half-etching of the roots of interconnected terminals of interconnected lead frames.

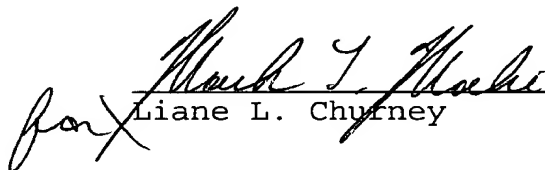
Independent Claim 11 is directed to a frame for forming individual semiconductor packages, and recites "each said lead frame having a metal lead which defines a boundary between said lead frame and an adjacent said lead frame, and pairs of terminals project in opposite directions from each said lead disposed between an adjacent pair of lead frames, each said terminal having a root disposed closely adjacent and projecting from the corresponding said lead, and each said root being recessed inwardly on opposite sides thereof to define a hollow between laterally adjacent pairs of roots of the individual lead frames such that a maximum distance is maintained therebetween". Mclellan does not teach or suggest such a hollow as defined in Claim 11. Further, as mentioned above, Ebihara teaches hollows and openings defined within the die pad or body 1, and does not suggest any desirability of providing such a hollow between laterally adjacent pairs of roots of a lead frame. Accordingly, no combination of Mclellan and Ebihara would result in the invention defined in Claim 11.

Claims 12-16 depend on Claim 11 and are believed allowable therewith. Further, Claims 12-16 recite additional features which distinguish over the cited references. For example, Claim 12 recites "said hollows defined between laterally adjacent pairs of roots of the individual lead frames each additionally extend into a portion of the corresponding said lead which extends transversely between each laterally adjacent pair of roots". Neither Mclellan nor Ebihara disclose such a structure.

The Information Disclosure Statement submitted herewith cites several references for the Examiner's consideration. Pending Claims 1-16 are believed to patentably distinguish over the enclosed references, as none of these references are believed to teach or suggest the configuration of the frame recited in independent Claims 1, 3, 4 and 11.

In view of the above, the instant application is believed to be in condition for allowance, and action toward that end is respectfully requested.

Respectfully submitted,

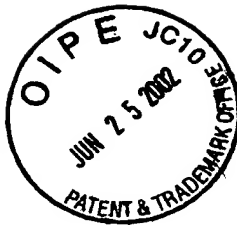
  
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Encl: Marked-up Substitute Specification  
Substitute Specification  
Marked-up Claims 1-3  
Marked-up Substitute Abstract of the Disclosure  
Clean Substitute Abstract of the Disclosure  
Letter to Official Draftsperson including  
Figures 1-6 with amendments indicated in red thereon  
Priority Document Transmittal, and Claim of Priority  
including enclosures listed thereon  
Letter Transmitting Supplemental Declaration and  
Supplemental Declaration  
Information Disclosure Statement including  
enclosures listed thereon  
Postal Card

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FRAME FOR SEMICONDUCTOR PACKAGE INCLUDING PLURAL LEAD  
FRAMES HAVING THIN PARTS OR HOLLOWES ADJACENT THE TERMINAL  
ROOTS

#### BACKGROUND OF THE INVENTION

##### 1. Field of the Invention

[0001] The present invention relates to a frame for semiconductor package or packages in which a semiconductor device is mounted on a lead frame and the outside thereof, particularly the upper surface of semiconductor device, is encapsulated with molding compound.

##### 2. Description eof the Prior Art

[0002] In recent years, it has been required to miniaturize and shape a semiconductor product mounted on a substrate so as to be thinner, as the packaging of the semiconductor is made ~~denser~~ more dense. It has been ~~severely~~ required for LSI to reduce the number of chips by improving integration level and to miniaturize and make a package lighter. The ~~popularization~~ popularity of so-called CSP (Chip Size Package) is rapidly ~~advancing~~ increasing. Particularly, in the development of a thin semiconductor product with a lead frame, the semiconductor package of the single side encapsulation type has been developed in which a semiconductor device is mounted on a lead frame and the surface of the semiconductor device mounted on a lead frame is encapsulated with molding compound.

[0003] Fig. 1 is a sectional view of one example of a semiconductor package. Fig. 2 is a plan view thereof. The

semiconductor package shown in Figs. 1 and 2 is comprised of a lead frame 1, a semiconductor device 4 mounted on a die-pad 3 supported with suspending leads 2 of lead frame 1, metallic thin wires 6 electrically connecting electrodes provided on the top face of the semiconductor device 4 with terminals 5 of lead frame 1, respectively and molding compound 7 for encapsulating the outside region of semiconductor device 4 including the upper side of semiconductor device 4 and the lower side of die-pad 3. The semiconductor package is of the non-lead type in which so-called outer leads ~~are~~ do not project ~~project~~ from the semiconductor package and ~~the~~ two of the inner leads and outer leads are integrated into terminals 5, wherein ~~used~~ lead ~~frame~~ frame 1 is half-cut by etching in such a manner that die-pad 3 is positioned higher than terminals 5. Since such a step is formed between die pads 3 and terminals 5, molding compound 7 can be inserted into the lower side of die-pad 3 so that a thin semiconductor package can be realized even though the semiconductor package has a non-exposed die-pad.

[0004] Since the semiconductor device is miniature, a matrix type frame is mainly used for the above-mentioned semiconductor package of the non-lead type, in which plural semiconductor devices are arranged in a direction of a width of the matrix type frame. Further, recently, ~~from~~ due to a demand for lower cost ~~down~~, ~~it is one~~ thought is to switch ~~over~~ from a frame of the individually ~~molding~~ molded

type shown in ~~Fig. 3~~Fig. 3(A) to a frame of the  
collectively ~~molding~~molded type shown in ~~Fig. 4~~Fig. 4(A).

[0005] In the frame of the individually ~~molding~~molded type, as shown in Fig. 3(A), individual molding cavities C of small size are provided separately within a frame F. After molding, individual semiconductor packages are stamped out so that semiconductor packages S shown in Fig. 3(B) are obtained. Namely, semiconductor devices are mounted on die-pads of lead frames through silver paste and others, and wire bonding is carried out. Thereafter, respective semiconductor devices are individually molded with molding compound and the respective molded semiconductor devices are stamped out to form individual semiconductor packages.

[0006] In the frame of the collectively ~~molding~~molded type, as shown in Fig. 4(A), some molding cavities C of large size are provided within a frame F. Multiple semiconductor devices are arranged in a matrix formation within each molding cavity C, respectively and collectively molded with molding compound. Thereafter, the collectively molded semiconductor devices are cut at grid-leads L by means of a dicing saw so that a semiconductor package S shown in Fig. 4(B) is obtained. Namely, semiconductor devices are mounted on die-pads of lead frames through silver pastes and others and wire bonding is carried out. Thereafter, plural semiconductor devices ~~arranged~~ are collectively molded with molding compound to a given cavity

size, and then the collectively molded semiconductor devices are cut to form individual semiconductor packages by dicing.

[0007] In the above-mentioned semiconductor package of the collectively ~~molding~~molded type, plural semiconductor devices are arranged in a matrix and collectively molded with molding compound. Thereafter, the collectively molded semiconductor devices are divided into individual semiconductor packages. In this case, the collectively molded semiconductor devices are cut at grid-leads by means of a dicing saw, while terminals of the lead frame are cut off from the grid-leads.

[0008] Generally, in the case of producing products by etching, parts designed to form a right angle are finished to have a roundish shape (R-shape), no matter how the etching process is carried out. In a frame for a semiconductor package of the collectively ~~molding~~molded type, even if connecting parts of grid-leads L with which define the terminals 5 of lead frame ~~is designed~~ frames are intended or designed to form ~~a-right angle~~ angles, products cannot be obtained as designed, since etched products have an R-shape as shown in Fig. 5. Further, as shown by the dotted line in Fig. 6, cut surfaces of terminals 5 of lead frame which are exposed in cut surface ~~after cutting of the~~ into form individual semiconductor packages (which are formed by dividing the collectively molded semiconductor devices at cut line  $\alpha$  by dicing) ~~becomes~~

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~~larger to approach to each other, in a case where larger~~  
because the R-shape is formed at the roots of terminals 5.  
Accordingly, a problem arises in that accident-of accidental  
~~short circuit is circuiting can be~~ caused by a soldered  
bridge.

#### BRIEF SUMMARY OF THE INVENTION

[0009] An object of the present invention is to provide  
a frame for a semiconductor package of the collectively  
~~molding~~molded type used for the production of semiconductor  
~~package packages~~, in which accidents such as a soldered  
bridge are prevented.

[0010] In order to achieve the above-mentioned object, a  
first type of frame for a semiconductor package of the  
present invention comprises plural lead frames arranged in  
a matrix through grid-leads, the grid-leads having  
terminals ~~projected~~projecting from the grid-leads, in which  
respective semiconductor devices are mounted on die-pads  
supported with suspending leads of individual lead frames,  
the semiconductor devices are collectively molded with  
molding compound, and the collectively molded semiconductor  
devices are cut into individual semiconductor packages at  
~~grid-frames~~leads, wherein thin parts are formed in areas  
corresponding to the neighborhood of the roots of  
individual terminals, the thin parts being formed by half-  
cutting ~~by or half--~~etching metal of the areas from the  
front or back thereof.

[0011] Further, a second type of frame for a semiconductor package of the present invention comprises plural lead frames arranged in a matrix through grid-leads, the grid-leads having terminals ~~projected~~projecting from the grid-leads, in which respective semiconductor devices are mounted on die-pads supported with suspending leads of individual lead frames, the semiconductor devices are collectively molded with molding compound, and the collectively molded semiconductor devices are cut into individual semiconductor packages at grid-frames~~leads~~, wherein hollows are formed in areas corresponding to the neighborhood of the roots of individual terminals.

BREIF DESCRIPTION OF THE DRAWINGS

[0012] Fig. 1 is a sectional view of one example of a semiconductor package.

[0013] Fig. 2 is a plan view of the semiconductor package shown in Fig. 1.

[0014] Figs. 3(A) and 3(B) are explanatory views of a frame of the individually ~~molding~~molded type.

[0015] Figs. 4(A) and 4(B) are explanatory views of a frame of the collectively ~~molding~~molded type.

[0016] Fig. 5 is an explanatory view of an R-shape generated by etching.

[0017] Fig. 6 is an explanatory view showing a state where cut surfaces of the terminals are exposed ~~in cut surface of collectively molded semiconductor devices~~.

[0018] Fig. 7 is a plan view of one example of a first type of frame for a semiconductor package of the present invention.

[0019] Fig. 8 is a partial enlarged view of the frame shown in Fig.7.

[0020] Fig. 9 is a sectional view taken on line A-A in Fig. 8.

[0021] Fig. 10 is a partial enlarged plan view of one example of a second type of frame for a semiconductor package of the present invention.

[0022] Fig. 11 is a partial enlarged plan view of another example of a second type of frame for a semiconductor package of the present invention.

#### DETAILED DESCRIPTION

[0023] ~~Then, referring~~Referring to the figures, embodiments of the present ~~inventions~~invention are explained. Fig. 7 is a plan view of one example of a first type of a frame for a semiconductor package of the present invention. Fig. 8 is a partial enlarged plan view of the frame shown in Fig. 7. Fig. 9 is a sectional view taken on line A-A in Fig.8.

[0024] In these figures, F designates a metal frame for lead frames, in which lead frames 10 are arranged in a matrix of 3×4 through grid-leads L. The grid-leads L connect terminals ~~11~~5 of adjacent lead frames 10 with each other. As shown in Figs. 8 and 9, areas ~~including~~in the neighborhood of the roots of terminals connected ~~with~~by

grid-leads L are provided with thin parts 11 which are formed by half-cutting by etching the metal of the areas. The thin parts 11 are formed to the outside of cut lines  $\alpha$  cut by means of a dicing saw. Therefore, even if R-shapes are generated at the roots of terminals 5, R becomes smaller by an extent of that the thickness of metal of the areas is decreased, as compared with that of the areas being which are not half-cut by etching. Accordingly, a sectional area of terminals 5 cannot be increased at cut lines  $\alpha$ .

[0025] ~~Process~~ A process for producing semiconductor packages using the frame F is as follows. First, semiconductor devices are mounted on die-pads 3 of the respective lead frames 10 of frame F through silver pastes and wire bonding is made between terminals 5 of lead frames and electrodes provided on the top face of semiconductor devices. Thereafter, twelve semiconductor devices are collectively molded with molding compound to a given cavity size and then the collectively molded semiconductor devices are cut at grid-leads L by means of a dicing saw in such a manner that terminals 5 of individual lead frames are left, by which the collectively molded semiconductor devices are divided into individual semiconductor packages.

[0026] In the individual ~~frame for~~ semiconductor package produced, the area of the terminals 5 which are exposed ~~in at the cut surfaces~~ surfaces of mounted molded resin cannot be increased. Accordingly, sufficient intervals are

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~~kept~~maintained between adjacent terminals 5, ~~into~~ such an extent that accidents such as a soldered bridge are prevented.

[0027] In the above-mentioned example, half-cut parts are formed on the front side ~~at~~in the neighborhood of the roots of terminals connected with grid leads. However, even if half-cut parts are formed on the backside by half-cutting ~~by etching~~or half-etching metal from the backside, the half-cut parts formed on the backside have the same effect.

[0028] Fig. 10 is a partial enlarged plan view of one example of a second type of frame for a semiconductor package of the present invention.

[0029] The frame is provided with hollows 12 having an angular shape ~~at~~in the neighborhood of the roots of terminals 5. The hollows 12 are formed ~~to the~~ outside of the cut line. If hollows 12 having such a shape are provided at the roots of terminals 5, problems caused by the R-shape formed at the roots of terminals by etching are solved. Accordingly, ~~sectional~~sectional areas of terminals 5 are not increased.

[0030] Fig. 11 is a partial enlarged plan view of another example of a second type of frame for a semiconductor package of the present invention.

[0031] The frame has round hollows 12 at the roots of terminals 5. The hollows 12 are formed in such a manner that the hollows cut into a part of grid-leads L from cut

line  $\alpha$  along which the frame is cut. In the case where hollows 12 having such a shape are provided at the roots of terminals 5, problems caused by the R-shape formed at the roots of terminals by etching are also solved. Accordingly, sectional areas of terminals 5 are not increased.

[0032] In the case of a semiconductor package produced using a second type of frame as shown in Figs. 10 and 11, sectional areas of terminals exposed at the cut surface of molded resin ~~does~~do not become larger, so that intervals between adjacent terminals 5 are sufficiently ~~kept~~maintained. Accordingly, accidents such as a soldered bridge do not occur.

[0033] As ~~mentioned above~~mentioned, a frame for semiconductor package of the present invention comprises plural lead frames arranged in a matrix through grid-leads, the grid-leads having terminals ~~projected~~projecting from the grid-leads, in which respective semiconductor devices are mounted on die-pads supported with suspending leads of individual lead frames, the semiconductor devices are collectively molded with molding compound, and the collectively molded semiconductor devices are cut into individual semiconductor packages at grid-~~frames~~leads, wherein thin parts are formed in areas corresponding to the neighborhood of the roots of individual terminals, the thin roots being formed by half-~~cutting by~~ etching metal of the areas from the front or back thereof. Alternatively, Or hollows are formed in areas corresponding to the

neighborhood of the roots of individual terminals.  
Accordingly, ~~it is inhibited that~~ increased sectional  
~~area~~areas of terminals ~~is formed~~are inhibited or prevented,  
so that intervals between adjacent terminals 5 are  
sufficiently ~~kept~~maintained. Accordingly, accidents such as  
a soldered bridge do not occur.

[0034] Although particular preferred embodiments of the  
invention have been disclosed in detail for illustrative  
purposes, it will be recognized that variations or  
modifications of the disclosed apparatus, including the  
rearrangement of parts, lie within the scope of the present  
invention.

FIG. 1  
PRIOR ART

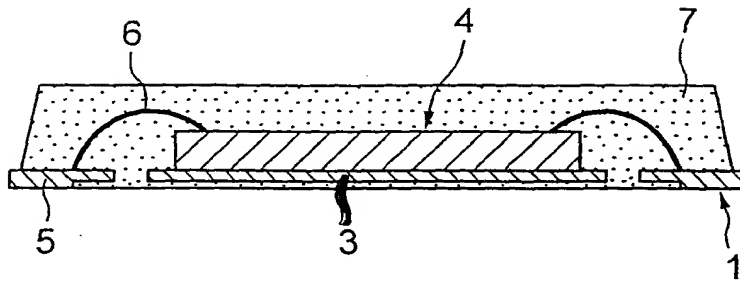
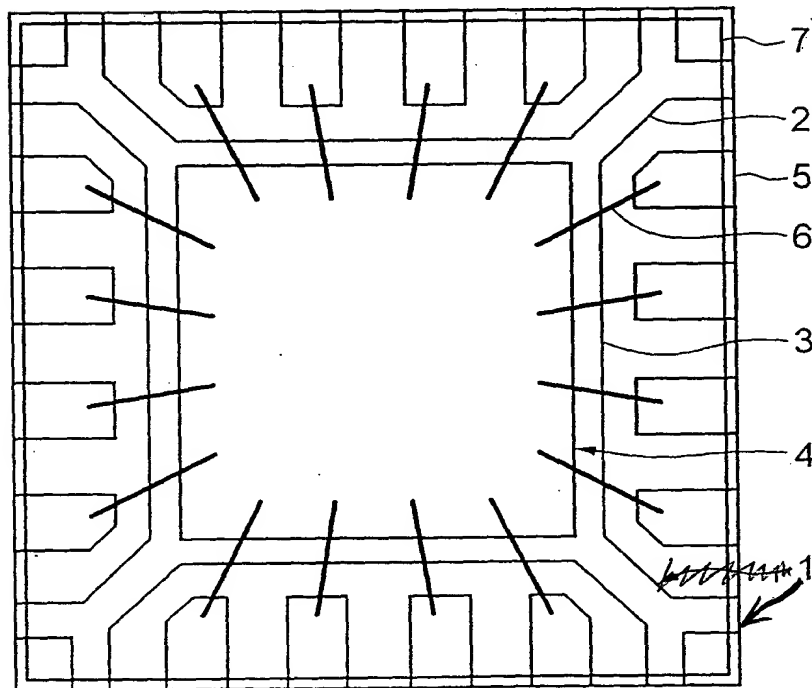


FIG. 2  
PRIOR ART



~~FIG. 3~~

FIG. 3(A)  
PRIOR ART

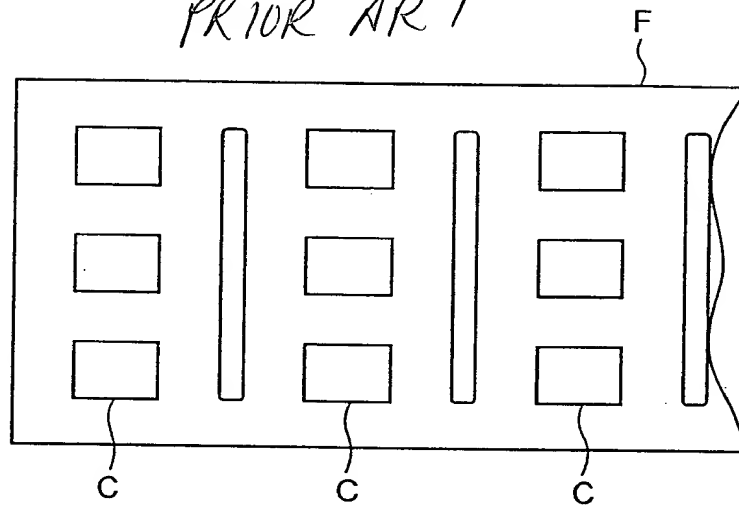
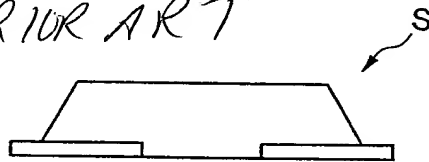


FIG. 3(B)  
PRIOR ART



~~FIG. 4~~

FIG. 4(A)

PRIOR ART

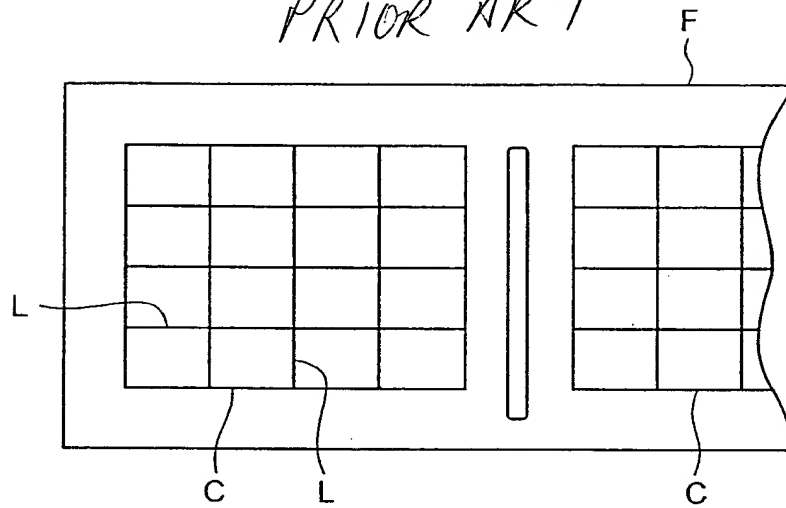


FIG. 4(B)

PRIOR ART



FIG. 5

PRIOR ART

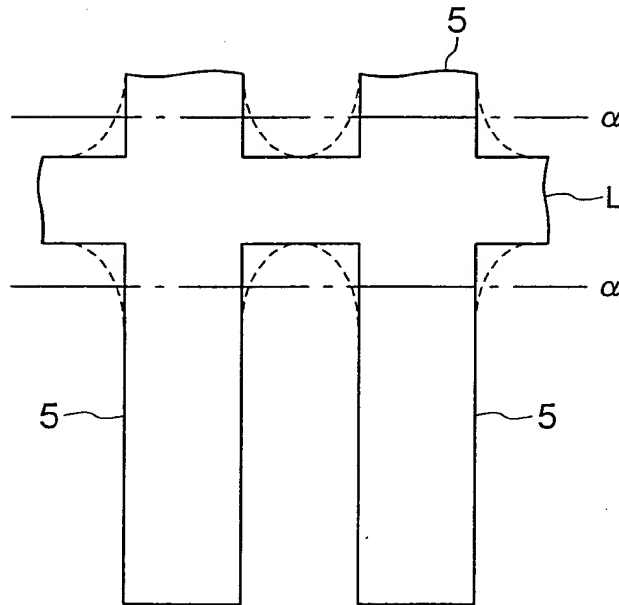


FIG. 6

PRIOR ART

